

REMARKS

The Office Action of January 21, 2009 has been received and its contents carefully considered.

The Objections:

Section 3 of the Office Action objects to the drawings on the grounds that they must show every feature of the invention specified in the claims. The objection is respectfully traversed, since corrected drawings that add a dummy gate arrangement 9 in Figure 3(c) and a new Figure 4 were filed along with an Amendment dated March 24, 2008. It is therefore respectfully submitted that the drawings now adequately show all of the features recited in the claims, so the objection should be withdrawn.

A related objection appears in section 4 of the Office Action, which alleges that the corrected Figure 3(c) and new Figure 4 represent new matter, as does an Amendment to the specification referring to the dummy gate arrangement 9. The Office Action comments, "specifically, there is nothing in the original disclosure which supports there being a structure remaining in the non-doped polysilicon region after the described etching process." The Office Action requires cancellation of the alleged new matter.

The objection and the requirement are respectfully traversed. It would appear that a clear issue has now developed with regard to the new matter objection, so a Petition is being filed concurrently to seek review of the objection. In order to ensure that the present paper is fully responsive to the Office Action, though, the arguments presented in the Petition will be repeated below. Basically, the fact that the application refers to dummy gate patterns that are disposed on the mask, that the application also advises that non-doped polysilicon has an etching rate that is faster than that of P-doped polysilicon but slower than that of N-doped polysilicon, and that the application refers (an original claim 1, for example) to a dummy gate in addition to N type and P type gates (which might be characterized more accurately as "gate electrodes") implies that a dummy gate electrode should be shown in Figure 3(c), and the region marked by reference number 6 in Figure 3(b).

The present application discloses a technique for confronting a problem that arises when N type polysilicon gate electrodes and P type polysilicon gate electrodes are etched

simultaneously. The problem is illustrated in Figure 2 of the application's drawings, which shows that some of the gate electrodes are over-etched, resulting in gate electrodes that are tapered by the time other gate electrodes are completely etched. The solution to this problem is summarized in the paragraph bridging pages 4 and 5 of the present application. This paragraph states, "The present invention aims to provide a semiconductor device comprising an N type polysilicon gate and a P type polysilicon gate both disposed simultaneously, wherein a dummy gate made of non-doped polysilicon is disposed for polysilicon gate etching and set so as to take an area larger than the total area of the N type polysilicon gate and the P type polysilicon gate ...".

In the original version of Figures 3(a)-3(c), phosphor ions are implanted into a region 4 for forming an N type gate electrode and boron ions are implanted into a region 5 for forming a P type gate electrode. No impurities are injected into a dummy gate electrode region 6. Subsequent processing results in gate electrodes as shown in Figure 3(c), but a dummy gate electrode is not shown in the original version of Figure 3. It is Applicant's position that an ordinarily skilled person who had read the present application would have realized that a dummy gate electrode should be shown in Figure 3(c), in the dummy gate electrode region 6, and that an ordinarily skilled person who had read the application as-filed would have realized that the inventor was in mental possession of the alleged new matter. However, section 4 of the Office Action of January 21, 2009 asserts that "there is nothing in the original disclosure which supports there being structure remaining in the non-doped polysilicon region after the described etching process." Applicant respectfully disagrees with this assertion.

The present application discloses that P type polysilicon and N type polysilicon etch at different rates (see, for example, the paragraph bridging pages 2 and 3 of the application and the paragraph bridging pages 7 and 8). The application also discloses that non-doped polysilicon etches at a rate which lies between the etching rate of P type polysilicon and N type polysilicon (see the paragraph at page 7 of the application, lines 14-25). Since both a P type polysilicon gate electrode and an N type polysilicon gate electrode are shown in original version of Figure 3(c), what the application calls a "dummy gate" of non-doped polysilicon should also be present in Figure 3(c), within the region identified as dummy gate electrode region 6 in Figure 3(b).

Furthermore, although the drawings do not show a mask with patterns for etching the N type and P type gate electrodes that are shown in the original version of Figure 3(c), an ordinarily skilled person would have understood that a mask is used to permit etching of these gate electrodes. The application advises that dummy gate patterns are disposed on the mask (see page 7, lines 3-7). An ordinarily skilled person would have realized that the result would be a dummy gate electrode in Figure 3(c), as in the replacement drawing sheet that was forwarded with the Amendment filed on March 24, 2008.

The application discloses that the dummy gate has an area larger than the total area of the N-type polysilicon gate and the P-type polysilicon gate (see the paragraph, noted above, bridging pages 4 and 5 of the application). This is what is shown in new Figure 4.

The new matter allegedly added to the specification includes the following sentence that was modified by the Amendment filed on March 24, 2008: "Subsequently, patterning is done by a lithography technique and the ~~non-doped polysilicon~~ and doped polysilicon regions 4 and 5 ~~[[in]]~~ and the dummy gate electrode region 6 are etched to form gate electrodes 7 and 8 and a dummy gate arrangement 9 (see Fig. 3(c))." The alleged new matter added to the specification also includes the following modification that was presented in an Amendment filed on April 27, 2006: "Fig. 3(c) shows that the area occupied by the etched non-doped polysilicon ~~region 6~~ dummy gate pattern is larger than the total area occupied by the N-type and P-type polysilicon ~~regions~~ gates which have been etched." From the above discussion of the drawing changes, it will be apparent that these modifications to the specification were within the mental possession of the inventor at the time this application was filed.

The Rejection on the Prior Art:

Section 7 of the Office Action rejects all of the pending claims for obviousness based on US patent 5,783,850 to Liao et al, US patent 6,541,359 to Gabriel et al, and US patent 5,665,203 to Lee et al, along with evidence provided by another patent. These references will hereafter be called simply "Liao," "Gabriel," and "Lee." For the reasons discussed below, it is respectfully submitted that the inventions defined by the independent claims would not have been obvious from these references.

Independent claim 3 provides that a first region of a polysilicon layer is implanted with N type ions, a second region is implanted with P type ions, and a further region is left non-doped. Claim 3 then recites the step of “simultaneously gate-etching an N type polysilicon gate electrode ..., a P type polysilicon gate electrode ..., and a non-doped polysilicon dummy gate arrangement ...”. Claim 3 also recites that “the non-doped polysilicon dummy gate arrangement has an area that is larger than the total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode.” Independent claim 15 includes similar limitations.

In contrast, the Liao reference merely shows a PMOS gate and an NMOS gate. The reference does not disclose the step of the simultaneously etching an N type region, a P type region, and a non-doped region. Nor does the reference disclose etching that results in an area occupied by a non-doped polysilicon gate arrangement being larger than the total area occupied by an N type gate and a P type gate.

Similarly, the Gabriel reference does not disclose simultaneous etching of an N type region, a P type region, and a non-doped region. Nor does the reference disclose etching that results in a non-doped polysilicon gate arrangement having an area that is larger than the total area occupied by an N-type gate and a P-type gate.

Although the Lee reference shows a two-step etching process, it does not disclose an etching process that results in an area occupied by a non-doped polysilicon gate arrangement being larger than the total area occupied by N type and P type gates.

Finally, the Lu reference also fails to show simultaneous etching of an N type region, a P type region and a non-doped region, or a non-doped polysilicon gate arrangement that is larger in total area than an N type gate and a P type gate.

Accordingly, the rejection for obviousness should be withdrawn.

The remaining claims depend from the independent claims discussed above and recite additional limitations to further define the invention. They are therefore automatically patentable along with their independent claims and need not be further discussed.

Conclusion:

For the foregoing reasons, it is respectfully submitted that this application is in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,

A handwritten signature in cursive script, reading "Allen Wood".

Allen Wood
Registration No. 28,134
Customer number 23995
Rabin & Berdo, P.C.
(202) 326-0222 (telephone)
(202) 408-0924 (facsimile)

AW/ng